AN EXPERIMENTAL TRANSISTORIZED TELEVISION SYNC GENERATOR WITH RMA TYPE OUTPUT

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Letter on front cover:

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[illegible] industrial use.

[illegible] [illegible] circuits used in sync generating [illegible] applied with the principle of duality to the transistor. However, the transistor has unique properties of its own which make it more desirable to design a sync generator around it than adapt it to conventional circuits. Transistorized units function quite well in television sync generators, but lack stability required of a commercial unit. Instability is due mostly to the following factors:

(1) Characteristics vary between units. This is particularly true of the negative resistance curve in point contact units, which determines to a large extent pulse width and free running blocking oscillator frequency.

(2) Extreme susceptability to crosstalk, voltage variation and temperature variation.

(3) An actual change in characteristics from day to day, and with use, so that timing varies and the unit must be reset frequently.

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The Princeton Laboratories demonstrated a transistorized television sync generator for Industrial Television and for the "Walkie-Lookie" in the fall of 1952. The Princeton circuits were not available to the author until after the unit described here was developed and tested at Camden. Curiously, the two circuits bear little if any, resemblance to each other.

The sync generator described here was developed as a source of RMA type sync pulses for Industrial Television units. As such, it provides a vertical pulse 900 microseconds wide and a horizontal pulse 11 microseconds wide to the camera unit for synchronizing and blanking. In addition it adds the standard RMA synchronizing pulses to these blanking pulses in a separate output for combining with the previously blanked video signal.

In order to provide a unit small enough to fit existing ITV 5 and ITV 6 monitor cases, the sync generator had to be approximately the size of the existing non standard units. At the same time, the greater complexity of the RMA type pulses placed rigid restrictions on the circuit. The circuit described here was selected as the simplest possible, consistent with making all times adjustable to fit the RMA specifications and a minimum of component parts.

In designing this circuit, only the available TA169K transistor could be used. There were no junction types available at the time. In order to place as few restrictions on components as possible, no inductances or transformers are used. The smallest possible potentiometers, resistors, and condensers were used, not always with satisfaction. Crosstalk between units, and components far out of tolerance, were serious problems. The transistors themselves were often a bigger problem. Since they do not have uniform negative resistance curves, and hence will give different pulse widths and free running times in the same circuit, they are not completely interchangeable. The transistors used here were picked for performance in each functional unit.

frequency source. It is a crystal controlled unit (ref. a) which depends on the series resonant characteristic of the crystal for positive feedback in the oscillator circuit. The output of this oscillator drives three other circuits, the serration pulse generator, the 2/1 count down and the 7/1 count down transistors. It was intended to provide a second or free running mode for this transistor which was frequency controlled by the 60 cycle line in an AFC circuit. Time did not permit this "line lock" feature to be added, though circuits for it were described by Princeton Laboratories (ref. b).

The 7/1 count down unit drives the count down chain, with the final output at 60 cycles. The 2/1 count down unit provides the 1 H frequency and interlacing feature. The remainder of the transistors are switching units to time and steer pulses which trigger a blanking bit register and a sync bit register whose outputs are added to give the composite sync pulse.

Analysing the RMA sync signals, except for the vertical blanking period which is 900 microseconds in duration, the pulses consist of a 5 microsecond sync pulse delayed 1.8 microsecond and superimposed on an 11 microsecond blanking pedestal. During the 900 microsecond period this structure changes. The blanking pedestal is 900 microsecond long with first ~ 192 microseconds of 2.5 microsecond wide pulses at a 2 H rate, then a series of 3 pulses 59 microseconds wide with 5 microsecond periods between them, followed by 192 microseconds of 2 H pulses 2.5 microsecond wide followed by up to 330 microseconds of 1 H pulses 5 microsecond wide.

There is a definite time relation between the starting and stopping of all pulses. If we designate the start of the serrating pulse, which is also the end of the 59 microsecond pulses, as t = 0 the other sync pulses form this relation in time:

Serration Stop	t	= 0
H blank pedestal	t	= + 3.2 microsecond
1 H and 2 H start (all starts)		= + 5.0 microsecond
2 H stop		= + 7.5 microsecond
1 H stop		= + 10 microsecond
H Blank off		+ 14.2

[illegible] The 2/[illegible] start occurs at t = 0. This start is used to trigger a [illegible] microsecond delay transistor which triggers the H blanking timer. The H blanking timer generates an 11 microsecond pulse which drives two units. The leading edge drives the horizontal blanking buffer and the trailing edge the blank stop generator. There will be no blanking pedestal unless the H blank timer is triggered, and then it can only be as wide as the timer permits. To get a 900 microsecond vertical blanking pedestal, the blank off transistor is prevented from pulsing by a 900 microsecond pulse acting thru a gating circuit. Since the last pulse received will be an "on" or start pulse, the bit will produce a pedestal until the 900 microsecond gate is off and stop pulses also come thru. Because the start pulses will serrate the Vertical blanking pedestal, they also are held off by gatin the buffer. These pulses are gated by the bit register itself in the on position, so that no more start pulses can be received until a stop pulse reverses the bit. This system is reliable and prevents getting the blanking bit out of phase.

The serration stop is also a timing circuit which has a 5 microsecond pulse. The leading edge triggers the sync bit to the off position, and the trailing edge initiates all sync pulse starts. The serration stop is not gated although it is needed only 192 microseconds each period. Normally it will have no effect because the bit is already in the off position, and if it is not, the serration stop serves as an emergency reset.

The trailing edge of the serration timer triggers the 1 H and 2 H starts. The 2 H start is used only during a 570 microsecond period at the start of the 900 microsecond vertical blank pedestal. During this time the 1 H pulses must be off. This is necessary because both the 1 H and 2 H pulses trigger their own stops and 1 H stops must be off during the serration period, or they will cause extra serrations to appear. The three gating transistors 192 microseconds, 192 microseconds and 570 microseconds, are used to delay the serration period 192 microseconds, time the serration period, and time the 2 H on period respectively.

There are three stop and [illegible] start pulses, four of which are gated. Were it not for good waveform and the need for the serration period, the bit would be unnecessary since the timing pulses themselves are as wide as the pulses they generate in the bit register. All these pulses are applied thru diodes to prevent loading the transistors by the others in parallel.

The sync and blank outputs from the two bit registers may be added by a simple voltage divider connected between outputs. If even more sharply defined pulses and better clipping is desired, the pulses may be clipped in the transistor circuit shown, (fig. 2), or in a vacuum tube clipper-adder which is part of a unit to clip and combine sync and blanking pulses with video output from the cameras.

Figure 3 shows the oscillator, count down circuit, and gating pulse formers.

Referring to figure 3, the oscillator transistor oscillates by virtue of positive feedback thru the series resonant resistance of the crystal. This resistance is of the order of 5,000 ohms and imposes a restriction on transistor selection. The condition for oscillation is that:

$$\alpha_{ce} \geq 1 + \frac{R_x}{R_L} + \frac{R_x}{R_e} \quad \begin{pmatrix} \text{with R Base} \cong 0 \\ \text{see ref. a} \end{pmatrix}$$

Since $R_x = 5$ K and $R_L \cong 4.7$ K, with an R_e of 22K nominal, the transistor α_{ce} must exceed 2.27 if it is to oscillate. Because of this only about one TA165K in 10 will function in this circuit. Better results may be had with other transistors with a higher nominal α_{ce}. Figure 5 (a) and (b) shows the output waveforms. These are pulsed, not a sine wave, and thus ideal for use in trigger circuits. The 2/1 count and the serration timer are taken from the emitter, while the 7/1 count is taken from the base. This is done to prevent feedback from the 2/1 unit from giving larger even pulses than odd for the 7/1 count which will cause it to slip to 6/1 or 8/1 erratically. By using the separate tie points, no buffer is needed. The original circuit on which the criterion for oscillation is based had no resistor in the base circuit. The addition of this resistor reduces

[illegible]

The count down circuits are free running blocking oscillators which are chain triggered. The basic formulas for deriving the on and off times are given by McDuffie (ref. e). These are repeated here as approximations made after some simplifications and assumptions were made.

$$T_{on} \approx \frac{1}{B_h} \quad \text{where} \quad B_h = \frac{R_1 + R_{ee}}{R_1\, R_{ee}\, C}$$

$$\approx \frac{R_1\, R_{ee}\, C}{R_1 + R_{ee}} \qquad \text{but } R_{ee} = 400\,\Omega \text{ approximately}$$

$$T_h \approx \frac{R_1\, C\; 400}{R_1} \approx 400C \text{ seconds}$$

$$\text{and } T_L \approx \frac{1}{B_1} \approx \frac{R_{ee}\, R_1\, C}{R_{ee} + R_1} \qquad \text{where } R_{ee} \approx 100\text{ K}$$

$$\approx \left(\frac{100K\; R_1}{100K + R_1}\right) C$$

It should be noted from these equations that the ratio of "on" to "off" time is highly variable. These approximations assume a fixed base resistor of about 2.2 K. In practice it has been found necessary to use about 4.7K to prolong transistor life. The time varying resistor R_1 is a 100K potentiometer, which from the equation is seen to be in shunt with a 100K resistance Rec. With the equivalent parallel R thus determined, a value for C can be picked to give times equal to 7 or 5 or 3 counts somewhere near midrange on the potentiometer. This approximation is found to be surprisingly close. The only troubles encountered have been because of ceramic disc capacitors which either because they had capacity far in excess of their rated value, or a leakage resistance did not time as predicted. Changing to a paper or mica capacitor usually resulted in correct timing; trying several ceramic capacitors of the same marked value resulted in widely divergent times.

presence of the [illegible] resistor in the emitter. The on time is determined by the same formulas, except that it varies over about a 10/1 range with variations of base resistance. At 2.2 K the approximation formulas hold, thus using a 10K potentiometer as a base resistor, the maximum pulse width is about 3 times that indicated. However, it varies from transistor to transistor. Some units with a poor negative resistance curve will give a pulse only 1/10 as long as a better unit. Such transistors are best weeded out for use in the stop circuits and bit registers. Usually, but not necessarily, they also have low α_{ce} values as well. They will function in the bit registers if a matched pair is used.

Because this circuit is built in a small space, there is considerable cross talk between units running at the same repetition rate. Thus, all the monostable units which are supposed to trigger at $\not{t}$ times may trigger from cross talk at $t = 0$. Further, the voltage supplied from the battery may vary as much as one volt due to pulses acting in concert on its internal resistance. The effects of cross talk and voltage change are eliminated or reduced by the addition of a resistance between collector and emitter which raises the necessary trigger poten ial on the transistor. The value of this resistor was determined experimentally, there being no known way to calculate it. In general however, pulsing ceases if he resistor is below 180K. Crosstalk and feedback triggering cease if the value is somewhere between 270 and 470K. If this resistor is made too small pulse width and dependability is affected. If it is too large, the pulse will trigger at random from crosstalk.

The value of coupling condensers was also arrived at experimentally. If the condenser is too large, the monostable units will double pulse, if too small, pulsing will be erratic.

The monostable units are taken from the papers by A. W. Lo, (ref. d) and Harris, (ref. e). Where these circuits are used for delay by triggering from the back side of the collector pulse, RC differentiation is used to get first a positive and then a negative pulse. The following monostable unit responds only to the negative pulse.

[illegible] edge of [illegible] pulse [illegible]
[illegible] of the 2 H generator. Hurvic suggests this method, but goes on to recommend another. Lo uses an inductance to get a spike. Because this circuit is to represent economy and use a minimum of transistors and no inductances, both the above schemes are disregarded. This system appears very stable when once set up completely, but if any unit runs at random, or off time, it tends to pull other units by means of cross-talk.

The bit registers are basic transistor binary units which are not cross coupled for binary action, thus pulses are applied at one point for the "set" or "on" state, and at another point for the "off" or "reset" state. In the binary unit the two inputs are cross connected thru diodes so that a pulse reverses the state each time it is received.

In order to steer the pulses and bring them in when needed to trigger the bit registers, various gating circuits are used. In general, all gating circuits use a condenser and a germanium diode to control a pulse. Refer to figure 7. Assume we desire a negative pulse. The pulse can be put in at X and taken out at Y if (a) and (b) are tied to the same potential. If however, (a) is positive with respect to (b), the pulse amplitude must be greater to pass.

In this circuit, the gating pulses are obtained from the collectors of other transistors, nominally at 45 volts when off, and about 25 volts when on. Thus to off gate a negative pulse, (a) is connected to the collector and (b) to the -45 volt supply. To on gate, (b) is connected to the collector and (a) to a potential source about -35 volts.

The start gate for the 1 H pulses is more complex than this simple gate and deserves further explanation. The 1 H start gate has a voltage divider which holds the base of the diode at about -36 volts. The R and C values are picked so that the serrated pulse input from the collector is about 2.5 RC time. This gives a suitable negative pulse from the trailing edge of the collector pulse. Normally, the point of the diode is held at 45 volts which is sufficient to cut the diode off an no pulses pass thru it. When the 2/1 count unit is on, the RC circuit and diode to its collector carry the point up to

the bias potential [illegible]

period will trigger the 1 H start. The combined effect of RC discharge and the diode in the 2/1 collector prevent the 2/1 unit from triggering on its trailing edge.

In triggering the sync bit register, diodes are used to prevent loading as well as to gate the pulses. In some cases, where gate time is short and the pulse needed is small, the potential stabilizing return can be omitted and only a single resistor to the collector used. Where diodes are shunted, this is done to reduce their back resistance and keep the condenser from self biasing to cutoff.

The photographs show the output pulses as taken from the unit. Where deviations exist from RMA standards, as in rise time and overshoot, these are failings of the transistors and the circuits in which they are used. Any errors in timing or counts are due to adjustment, not to circuit failings. All timing factors are adjustable readily from the panel. Test points are available in the form of the back sides of solder tie points on the panel for checking waveforms at each point in the unit so that it need not be dismounted to check or adjust.

Due to the many crosstalk effects in the circuit, the combined outputs of the two bit registers do not yield a satisfactory RMA output. They must be clipped and added externally or by means of additional transistors not included in this unit. Time did not permit the additional work to be done.

Measurements made on a driven sweep oscilloscope show the pedestal and sync pulses to bear the proper time relationship to each other, and to be gated properly as required. Further work would be necessary to improve the long running time stability of the unit. Proper clippers and adders, and the 60 cycle "line lock" feature, remain to be added.

The TA165R Transistor has since been designated as the 2N32 for production.

(a) Crystal Oscillator - the Transistor - Bell Laboratories
Article by R. S. Carruthers - "Some Experimental and Practical
Applications of Transistor Oscillators.

(b) Princeton ITV sync generator paper - W. Pike, Second or Third
Quarter 1953 RCA Review

(c) McDuffie: Pulse Duration and Repetition rate of a Transistor
Multivibrator - Proc. I.R.E. November 1952 pp 1487

(d) Lo, A. W. - Transistor Trigger Circuits - Proc. I.R.E. - Nov. 1952 - pp. 1531

(e) Harris, J. R. - A Transistor Shift Register and Serial Adder -
Proc. I. R. E. - Nov. 1952 - pp 1597

Photograph #74724 shows the ITV-5 unit and camera with the transistorized RMA sync generator installed. The non standard sync generator normally used is shown at the bottom, and the transistorized version of it in the same chassis is shown at the right. The non standard sync generator uses 7 transistors, the RMA type unit 23.

Photograph #74725 shows the transistorized RMA unit below a studio rack which performs the same functions.

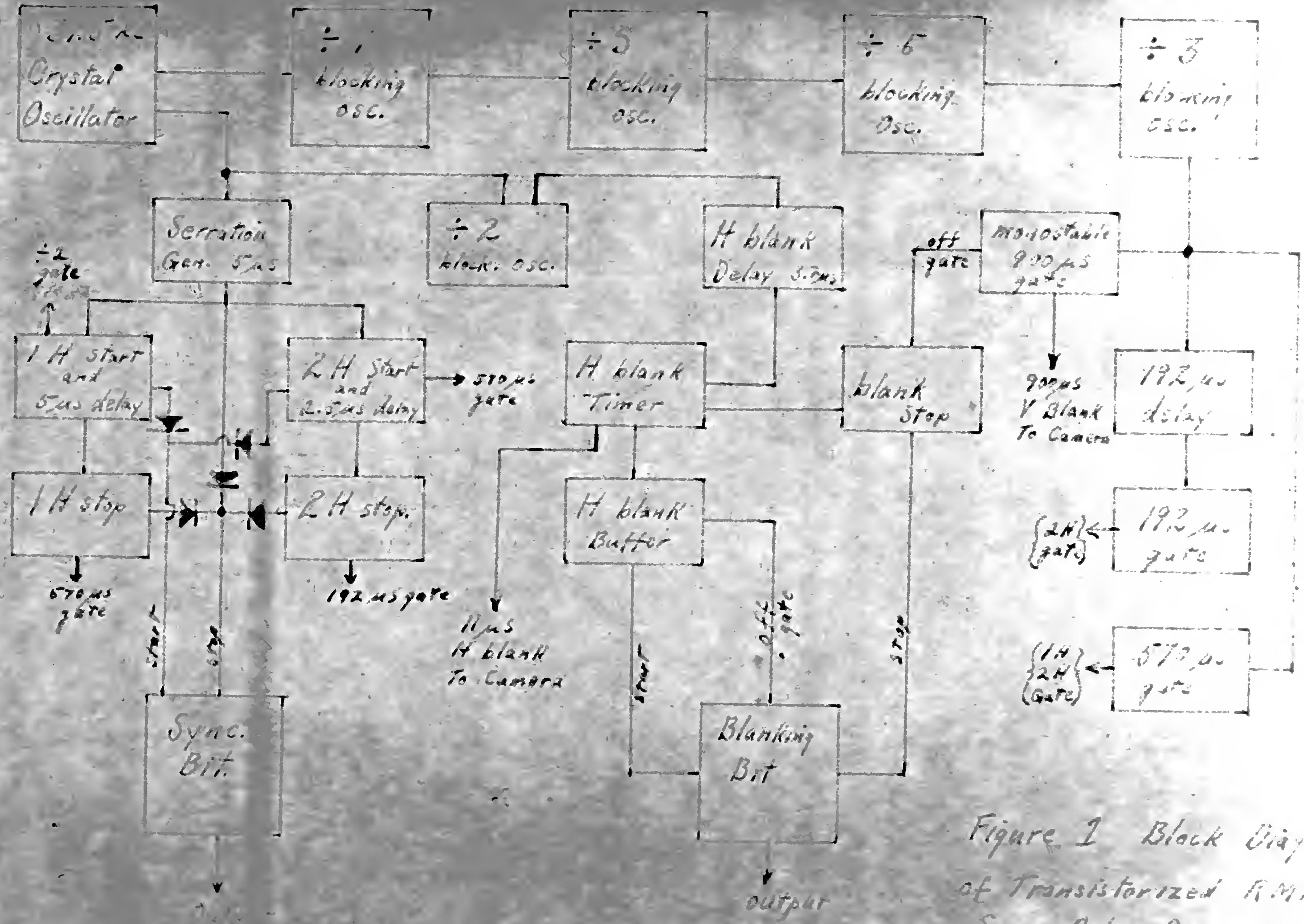


Figure I Block Diagram of Transistorized RMA Sync. Pulse Generator

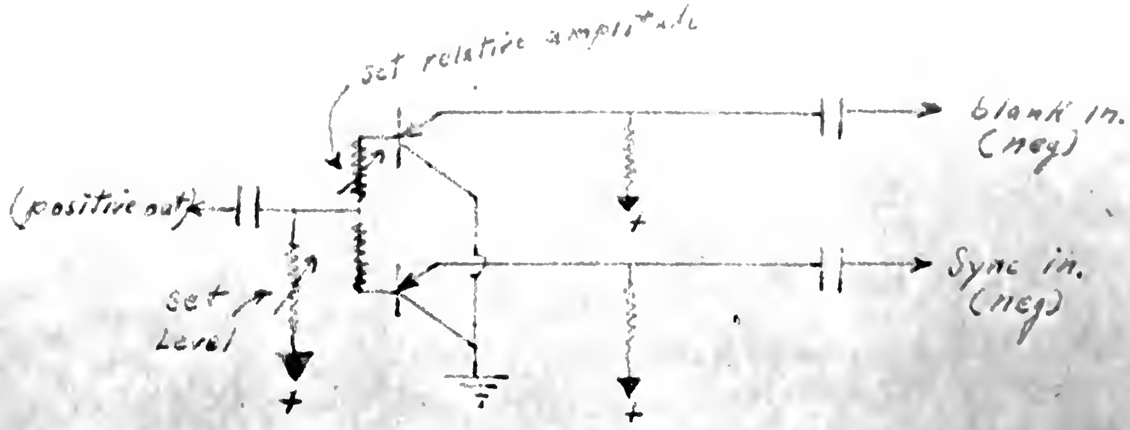


Figure 2. Transistor Clipper-Adder

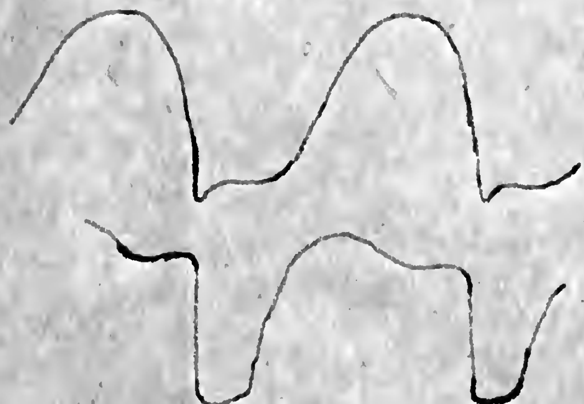


Fig 5(a) Crystal Oscillator emitter

Fig 5(b) Crystal Oscillator base

(These Waveforms vary considerably among different transistors. Limiting cases are pure Sine waves and pure pulses.)

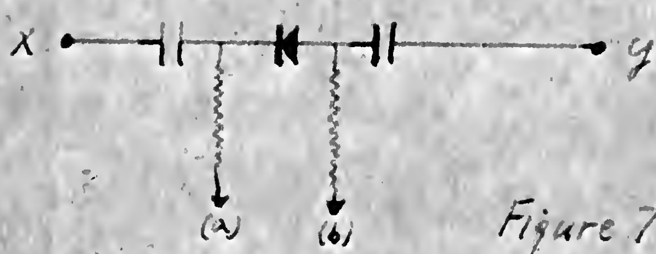


Figure 7. Basic Gate Circuit.

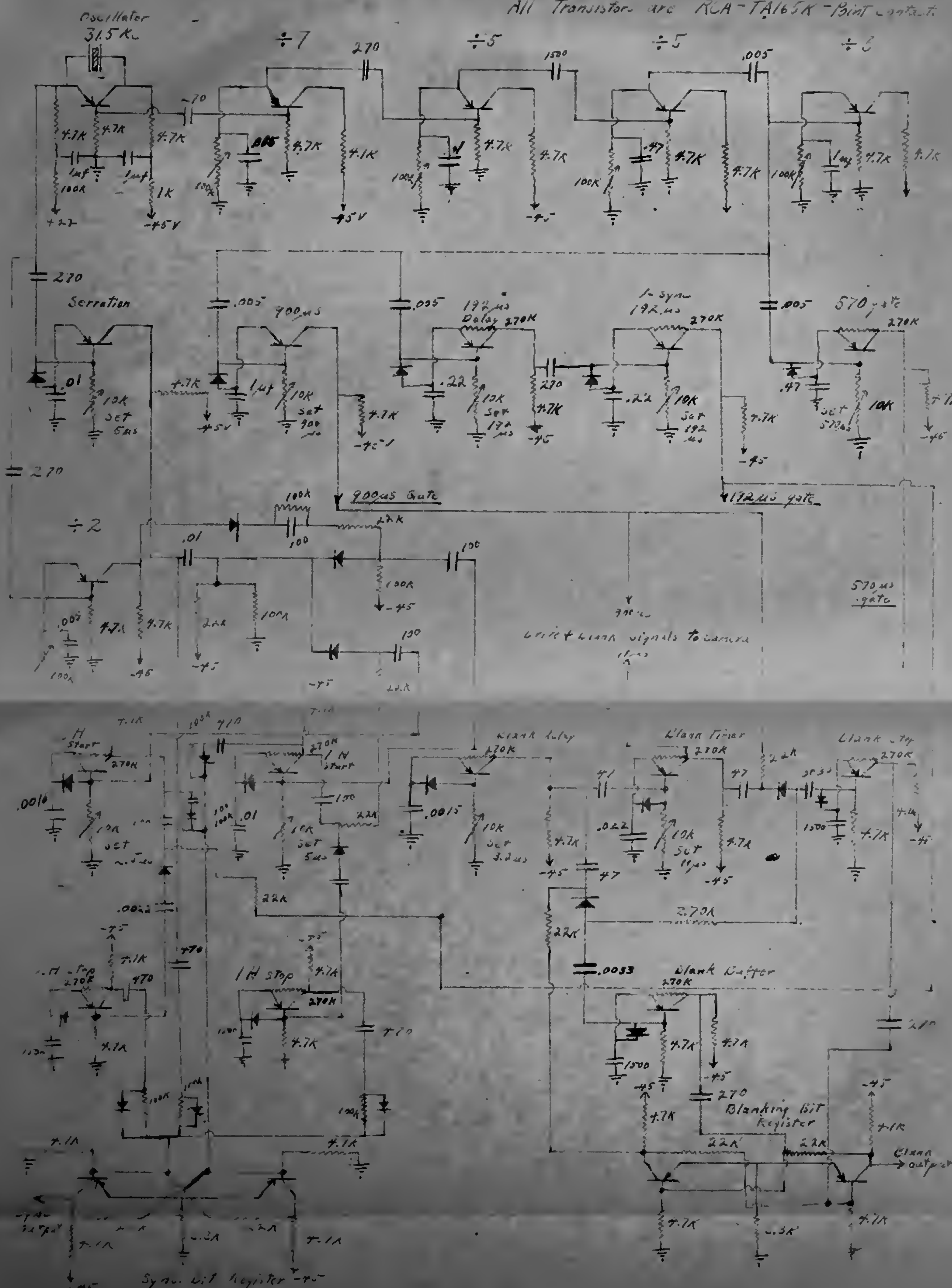


Figure 5 - Overall Schematic - RMA Type Sync. Generator

Figure 4 Sync. pulses from collector of Sync. Bit, one transistor removed. Serration stop, start, 1H stop and 2H stop pulses show.

Figure 6. Leading and trailing edge of serrating pulse taken at base of 2H start.

Figure 8. Collector pulses of 2/1 cpunt down

Figure 9. H blank stop pulse.The small pulse in front of it is crosstalk from the H Blank start pulse.

Figure 10. H blank timing pulse. 3.2 microsec. delay start is faintly visible ahead.

Figure 11. H blank start pulse. Trailing edge clutter is crosstalk from H blank stop.

Figure 12. H blank pedestal at bit register output before clipping. Note 3.2 microsecond delay shows ahead of this pulse. Presence of serration in the pulse renders it unfit for use without clipping.

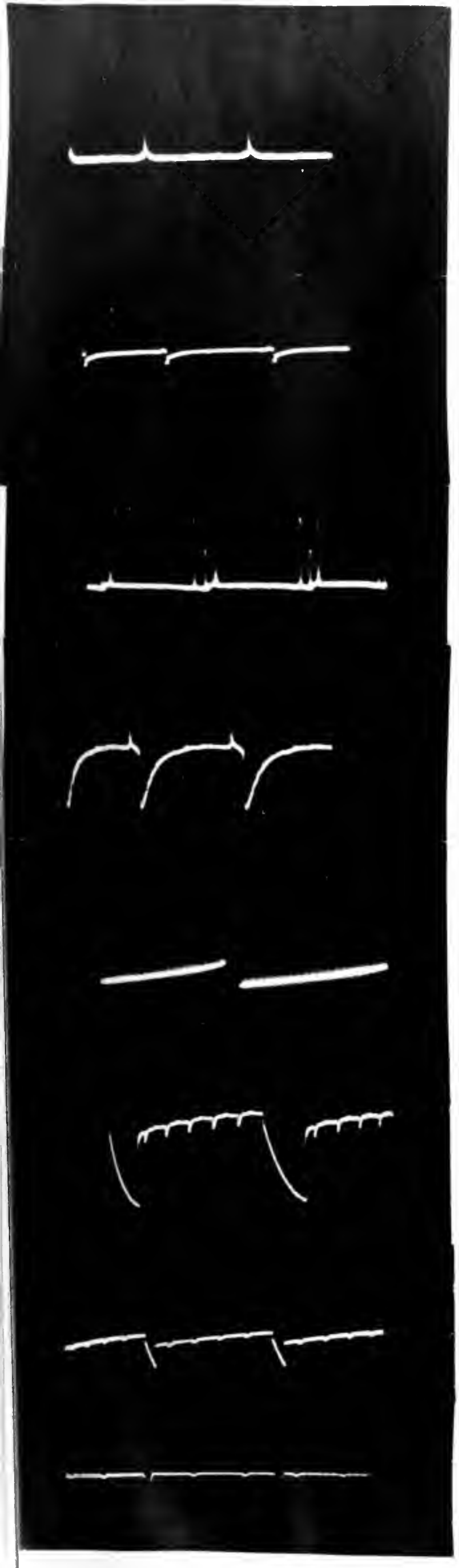


Figure 13. 2H stop pulse. 1 H stop is similar. Actual amplitude is about 20 v, but pulse width is so narrow it does not photograph.

Figure 14. Base of the 2H stop. The delay time is only faintly visible as a slight rise ahead of the more prominent drop.

Figure 15. Emitter of sync. bit register. Serration stop, starts and 1H stop show 2H stop is on such a short period it does not photograph.

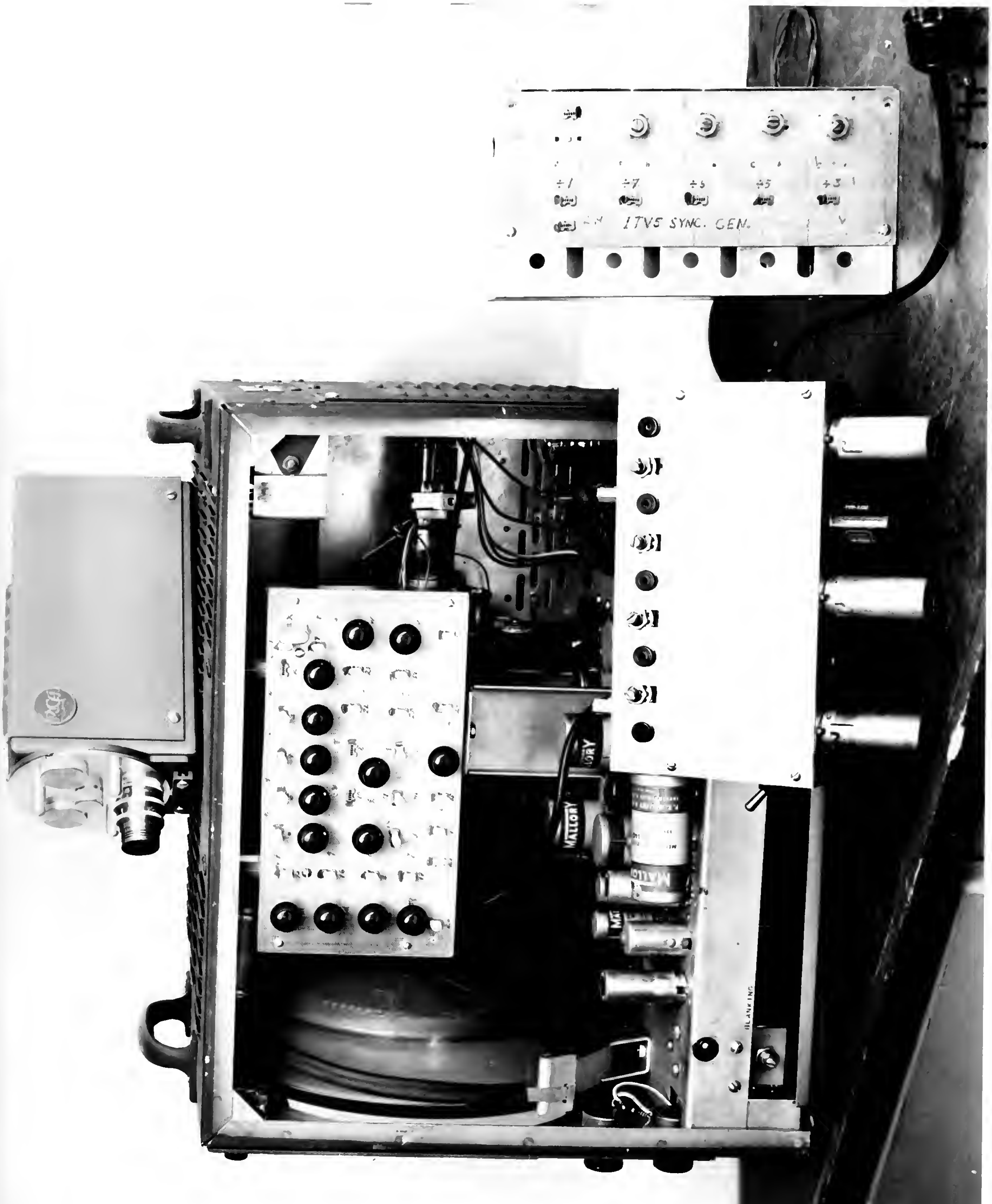
Figure 16. Serration delay taken in sync. start circuit.

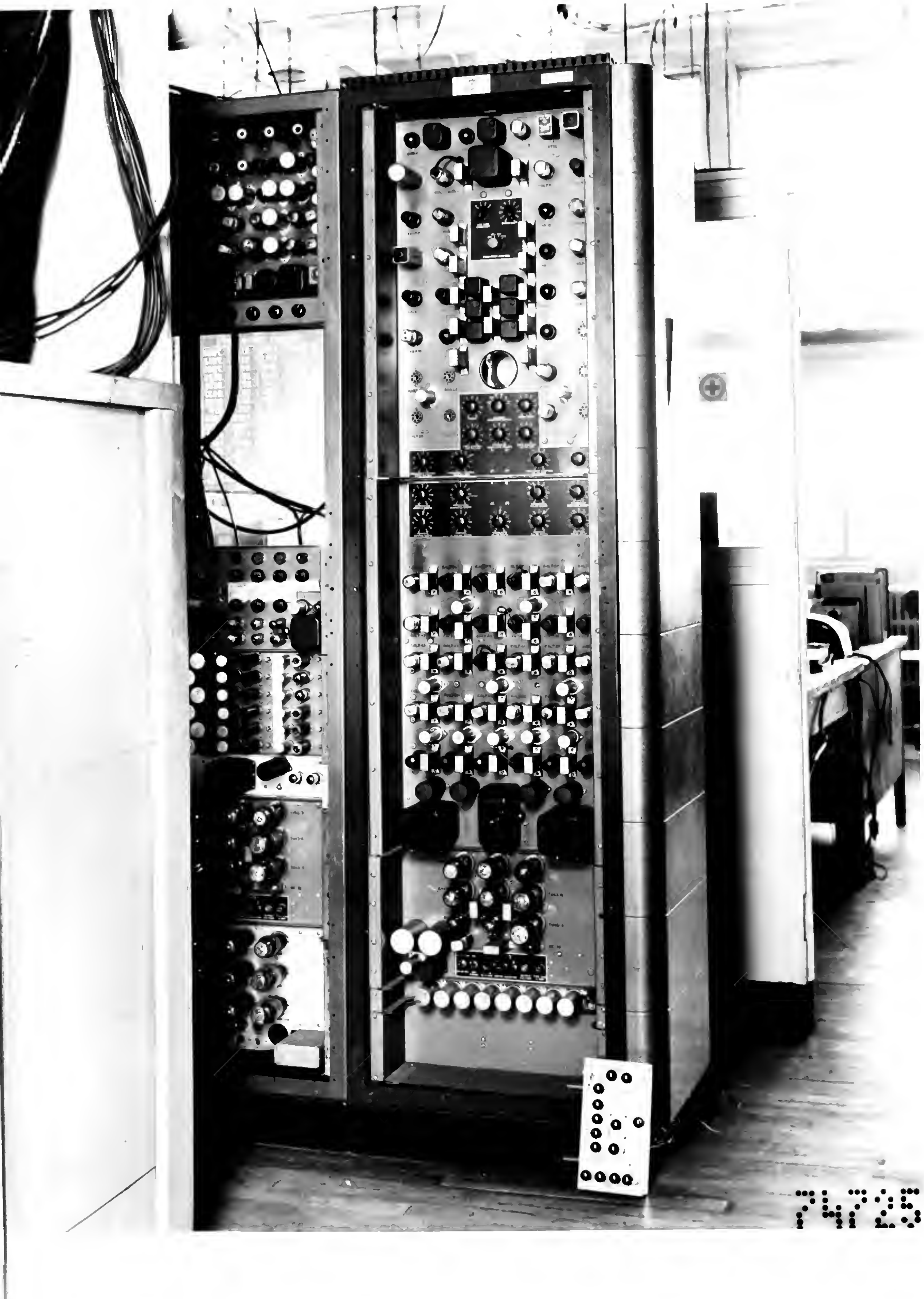
Figure 17. Trigger pulses to H blank stop showing 900 microsecond gate.

Figure 18. Seven to one count down taken at base of transistor. One count is lost in the wide base pulse.

Figure 19. Five to one count down.

Figure 20. Three to one count down.


ITV5 SYNC. GEN.
MALLORY
BLANKING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